# Memory – based Encoding Algorithm for Minimization of Inductive Cross-Talk based on Off- Chip Data Transmission

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**Abstract**— Inductive Cross-talk within IC Packaging is becoming a significant bottleneck in high speed inter chip communication. So the off-chip drivers typically source and sink 10 to 1000 drive internal loads. Thus simultaneously switching many off-chip drivers can cause large power (VDD) and ground current surges. These changes in current flow induce a voltage drop on the drivers' local VDD rail and a voltage rise on the drivers' local ground rail. The voltage drop is proportional to both the inductance of the VDD (ground) distribution network and the rate of change of the current flow (V= L * dI/dt).

In this work, we proposed a technique to avoid the inductive cross-talk in the inter-connect by encoding the data being transmitted off-chip. Bus encoding algorithms have been developed to overcome the capacitive cross-talk for on-chip buses, so the problem of on-chip capacitive cross-talk minimization for busses is very different from that of off-chip inductive cross-talk minimization. In this paper our approach also constructs cross-talk resistant CODEC algorithmically to utilize the memory-based CODEC solution.

Here we construct a set of equations which encoded the constraints that any legal vector sequence must satisfy to avoid supply bounce, signal glitching, and signal edge speed degradation. From this set of equations, we construct a set of legal vector sequences for the bus. We use this set to find the largest effective size of the bus that can be achieved by encoding, for a given physical size of the bus.

Our experimental results show that the proposed encoding based techniques result in reduced supply bounce and signal degradation due to inductive cross-talk, closely matching the theoretical predictions. As a result the overall delay of the bus actually decreases even after the use of the encoding scheme.

**Index Terms-** Bus Encoding algorithm, Delay, Inductive Cross-talk, Interconnect, Off-chip bus.

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## 1 INTRODUCTION

The limitation in package performance comes from the parasitic inductance and capacitance in the electrical interconnect [1, 3, 5] The parasitic inductance within IC packaging causes bounce on the power supply pins in addition to glitches and rise-time degradation on the single pins [1, 2, 10].In this work we give the mathematical analysis and the coding algorithm based on the reducing cross-talk for off-chip data transmission which we help on [1, 2]. This code is commonly referred minimization of inductive cross-talk for Off-chip data transmission based on encoding.

The first step in creating the bus expansion encoder is to create a set of constraints equations. [1, 3, 7]. The constraint equations are written so that arbitrary transitions can be evaluated for noise limit violations. When the transition is evaluated using the constraint equations and violates one of the user-defined noise limits, the transition is flagged as illegal and is removed from the set of data sequences that are allowed to be riven through the package interconnects. Each of the possible off-chip transitions are evaluated against each of the

constraint equations. The inductance factors that effect signal speed and integrity are as follows:-

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### 1.1 Supply Bounce Constraints

When a pin I in segment j is a VDD pin, it is required that the bounce magnitude due to the electrical parasitic in the package must not exceed the user-defined noise limit P supply. When the pin under evaluation is a VDD pin, a constraint equation is written to determine is any transitions that occur on the bus segment will result in a violation of P supply [1, 4, 6]. So the VDD pin in addition to any mutual inductive or capacitive coupling that occurs due to switching signals in adjacent pins. By multiplying the coupling magnitude by the transition value $v_i^j$ (which can be 0, 1, and -1). When the pin under evaluation is a VSS pin, a constraint equation is written to determine if any transitions that occur on the bus segment will result in a violation of P gnd. Typically supply (VSS and VDD) pins are interspersed at regular intervals between signal pins. Every nth pin is a VSS or VDD. The supply bounce is proportional to the number of pins switching low or high. Ground bounce is expressed as:

$$V_{bnc} = L\sum_i (di/dt)$$

Where L is the self inductance of the VSS pin and $\sum_i (di/dt)$ is evaluated over the number of signal pins switching low.

### 1.2 Glitch Magnitude Constraints

When a pin I in segment j is a signal pin, it is required that the coupled voltage onto that pin does not exceed any of the user-defined noise limit for signal coupling [9,11,13] if the signal pin is static $(v_i^j = 0)$ then the glitch magnitude onto the victim

pin must not exceed P0. As in the constraint equations for supply bounce, the magnitude of the coupling contribution of any neighboring pin is multiplied by the transition value V (Which can be 0, 1, or -1) of the neighboring pin.

If a signal pin j is static, then a glitch may be induced in its voltage due to neighboring pins which switch.

This is governed by the expression

## 1.3 Switching Speed Constraints

When a signal is switching, its transition can be speed-up if the coupled voltage induced by its neighbor's mutual inductance aids the transition. We would like that a signal is not slowed down (i.e. either speed-up, or un-integrated), in this transitions due to this effect we would like that when a signal j is rising (falling), the coupled voltage on this signal (equation 2) due to its neighbor's transitions is zero or positive or negative. In this way, the transitions of signals are not slowed down due to inductive cross-talk.

## 1.4 Rise time and Fall time Degradation Constraints

When a signal pin I in segment j transitions from logic 0 and logic 1, $(v_i^j = 1)$ it is required that the coupled voltage onto that pin does not hinder its rise time.

In a similar manner, when a signal pin I in segment j transitions from logic 1 to logic 0, $(v_i^j = 1)$ it is required that the coupled voltage onto the pin does not hinder its fall time.

Bus encoding algorithms have been developed to overcome the capacitive cross-talk for on-chip buses [8, 9, 10]. However the problem of on-chip capacitive cross-talk minimization for busses is very different from that of Off-chip inductive cross-talk minimization. Although our approach also constructs cross-talk resistant to [1, 8, 9], we utilize memory based CODEC solution [14].

In this work we proposed systematic encoding scheme to reduce inductive cross-talk.

## 2 OUR APPROACH

Consider a bus consisting of k identical segments, each of width n. For any segment j, let j-1 represent the segment to its immediate right. Let us also denote the values if the n bits of segment j as $v_i^j (0 \le i \le n-1)$. Figure 1 shows an example of

a bus configuration with k = 3 and n = 5. So the signal- to-power ratio for this bus configuration is 5/2 shown in figure1.

In general, when assigning package pins for an off- chip bus, VDD and VSS pins are interspersed among the signal pins in a regular fashion. The over all bus arrangement consists of a repetitive pattern of segments, each with their VDD and VSS pins in the same relative position within the segment which shown in figure 1.

In our approach, we write equations to encode the inductive cross talk constraints for all bits of the jth bus segment. The constraints are different for the signal, VDD and VSS pins. Depending of the number of neighboring pins whose mutual inductive effects we want to model, the constraint equations will include pins belonging to neighboring segments as well.

Since the segments are arranged in a repetitive manner, the encoding obtained for segment will be valid for all K segments within the bus. So here we used the valid sequences to construct a legal transition between bus vectors. From this digraph, we construct a memory – based CODEC which is used during the bus data transfer.

## 3   CODING ALGORITHM

If an m- bit bus can be encoded using the legal transitions in G, then there must exist a set of vertices $V_C \subseteq V$ , such that each $V_s \in V_c$ has at least 2m out going edges e ( vs , vd ) (Including the self edge), such that the destination vertex $v_d \in$ Vc. so the cardinality of Vc is at least 2m. Now for any given graph G, we find m by the following given Algorithm.

Initially m is taken n-1 (when n is physical length of the bus). So the input of this Algorithm will be m and G. Here we first, we find out- degree of each v (single vertices) $\in V$. If the out-degree of v is less than $2^m$ then we assigned $V \leftarrow V/v$ and delete all out- going edges rooted at V as well as all in- coming edges incident on v will continue this step until the graph is convergence. If after convergence the cardinality of v is greater than $2^m$, We can construct a memory- based encoder using the legal transition of G. In this case the effective bus size can be encoded in m. If m bit bus can not be encoded using G then we decrement m, we repeat this until we find a value of m such that the m bit bus can be encoded by G.

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Algorithm 1: Testing if G(V,E)can encode an n-bit bus
Encode (m, G(V,E)) where m=n-1 & n = size of bus.

1.   calculate the out degree $\forall v_i \in V$

2.   degree = 1

3.   Repeat steps 4 to 7 while degree=1

4.   degree = 0

5.   repeat steps 6 to 7 while each $v_i \in V$

6.   If (out-degree of $(v_i < 2^m)$ then
      $V \leftarrow V - v_i$ (where V is the set of vertices)
      $E \leftarrow E - e$ (where e is the edges which is inci-
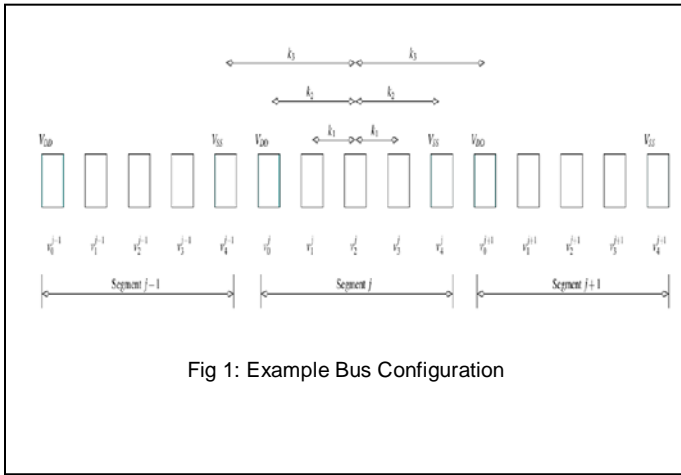      dent of $v_i$ )
      Set degree=1

7.   $v_i = v_i + 1$

8.   Exit

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Fig 1: Example Bus Configuration



Fig. 2 Encoding Efficiency

## 4 RESULT

In this work we encode an example bus configuration to avoid inductive crosstalk. The bus configuration is shown in figure1. Here we taken from Reference1, The first step consists of writing the constraint equations for every pin in the bus. In this bus r =7 k =3 and α=7/2. For the inductive coupling with a magnitude less than 0.08.This exercise yields 7 constraints equations shown below. Note that these constraints have been simplified by removing terms with $v_i^j = 0$

$$1.\; v_0^j = v_{DD} = \frac{z}{2}(no\,of\; v_i^j\; pins\,that\,are\,1) \le p_{bnc}$$

$$2.\; v_1^j = 1 \Rightarrow k1(v_2^j) + k2(v_3^j) + k3(v_4^j) + k4(v_5^j) \ge p_1$$

$$3.\; v_1^j = -1 \Rightarrow k1(v_2^j) + k2(v_3^j) + k3(v_4^j) + k4(v_5^j) \le p_{-1}$$

$$4.\; v_1^j = 0 \Rightarrow -p_0 \le k1(v_2^j) + k2(v_3^j) + k3(v_4^j)$$
$$+ k4(v_5^j) \le p_o$$

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$$17.\; v_6^j = v_{ss} = \frac{z}{2}(no\,of\; v_i^j\; pins\,that\,are -1 \le p_{bnc}$$

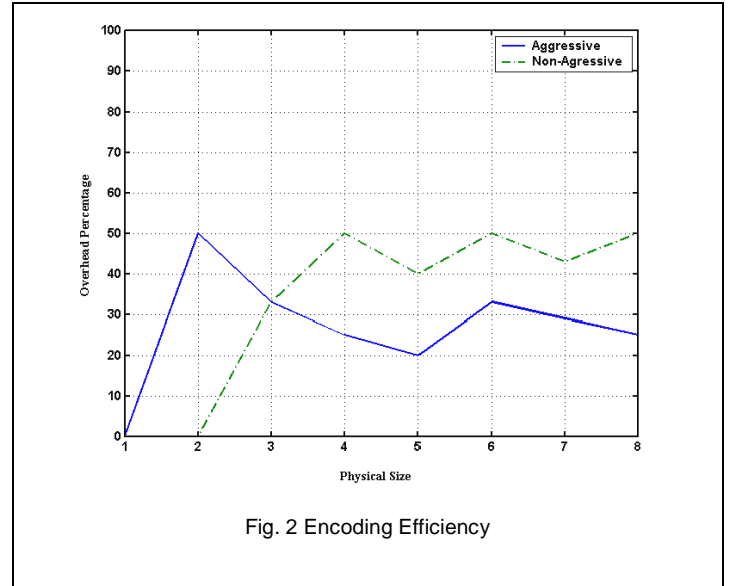## 5 CONCLUSION

In this work, we present encoding techniques which can help a designer trade off cross- talk against area overhead. Our experimental results show that the proposed techniques result in reduced delay variation due to cross- talk. As a result in reduced delay of a bus actually decreases even after the use of the encoding scheme. We also presented a technique to encode Off-chip bus data to avoid inductive cross –talk effects. The technique involves writing constraints equations which express the user-specified bounds on the amount of edge speed degradation, glitch magnitude, and supply bounce that can be tolerated. In this paper, we have introduce the concept of using data encoding to mitigate cross talk delay on buss and we presented a theoretical framework for understanding crosstalk immune coding. In this work we proposed a bus encoding technique to prevent cross talk delay for off-chip data. We incorporate all these inductive cross-talk effects in a common Mathematical framework. We construct a set of legal vector sequences with respect to of legal vector sequences with respect to inductive cross-talk, and use these to develop a CODEC for inductive cross-talk avoidance.

Our experimental results show that the proposed encoding based techniques result in reduced supply bounce and signal degradation due to inductive cross-talk, closely matching the theoretical predictions. As a result the overall delay of the bus actually decreases even after the use of the encoding scheme.

We found the value of the effective bus size n as a function of physical bus size m. the results are shown in figure 2, where we plot the bus size overhead (n-m / m) as a function of n.

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